



Bluetooth® Low-energy Integrated Module for SME's (BLIM4SME)

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Executive Summary

This document consists in the deliverable D5.2. “Final datasheet for RF IC, RF IPD Module and BLE Generic Module”. Its principle is to summarize specifications of the final results components and macro-components that are:

- The 2nd version of BLIM Testchip,
- The last version of IPD filter and antenna impedance matching,
- The BLIM module,
- The BLE Generic module.

The D5.2 is structured as follows:

- An introduction section for recall of general approach,
- Specification of 2nd version of BLIM Testchip,
- Specification of last version of IPD component,
- Specification of BLIM module,
- Specification of BLE Generic module.

Preamble

About the Project Results & terminology

For sake of readability of this document, and for respecting coherence with the DoW, the Project Results are summarized in this subsection (see also DoW table 3.2.2a). The correspondence with the technical/technology terminology used in this document is also provided (see also DoW section 1.1.2).

Result 1: BLE Generic Module:

This concerns in the BLE Generic Module in the form of a PCB that will embed the outcome(s) of Result 2 below, with additional features (e.g. bunch of sensors, etc).

The principal exploiter of this Result 1 is **PRISMA**.

Result 2: RF IPD Module:

This concerns the radio module that embeds IPD technology and which will be provided in two forms in the project:

- The **COTS module** which uses off-the-shelf radio components. Besides being a direct outcome of Result 2, it also serves for benchmark purposes for the **BLIM module** described below.
- The **BLIM module** which uses the BLIM4SME radio technology of Result 3 below.

The principal exploiter of this Result 2 is **NORDIC**.

Result 3: RF IC IP:

This concern the RF IC platform developed specifically in the project, and which is referred to as the **BLIM RF IC IP for the IP** and **BLIM testchip** for the implementation of the IP This outcome is in the form of a silicon IP which will be integrated in the project as a chip.

The principal exploiter of this Result 3 is **RW**.

1 Introduction

We defined a common **Generic Module**, c.f. section **Error! Reference source not found.**, with bunch of sensors, that can embed two types of communication modules: the **COTS Module** and the **BLIM Module**, c.f. section 5. Both of them are functionally and footprint-compatible. They even share same Cortex M0 MCU in order to share major part of their respective software. In addition, both communication modules are using same antenna and same IPD impedance matching and filter component, c.f. section **Error! Reference source not found.**. Both architectures are illustrated in Figure 1 below:

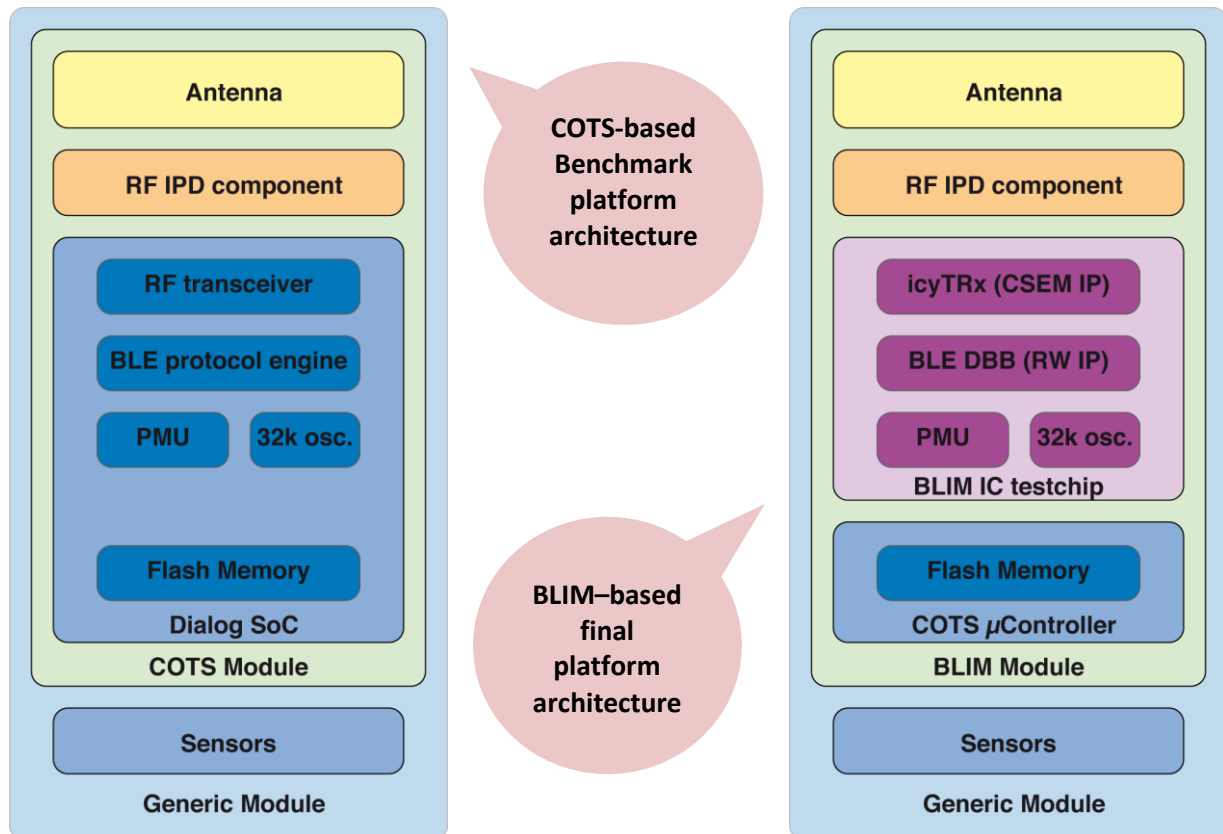


Figure 1: Bench platform and Final platform architectures

Main difference between benchmark platform and final platform is then the ensemble of specific components present on the **COTS Module** and **BLIM Module**, the later implementing the **BLIM Testchip**. This IC embeds CSEM icyTRx RF IP, implementing the Bluetooth® Low Energy PHY layer, with the RW BLE Core implementing the upper protocol layers.

Datasheets are described in following chapters associated to the different parts:

2. **BLIM Testchip** embedding the RF IC IP,
3. **RF IPD** component and associated antenna,
4. **COTS Module** and **BLIM Module**,
5. **Generic Module**.

2 BLIM RF IC IP

2.1 General description

The BLIM Testchip materializes the BLIM RF IC IP. It is intended to operate with a separate MCU supporting both software-related protocol part and application part, the whole implementing complete BLE application.

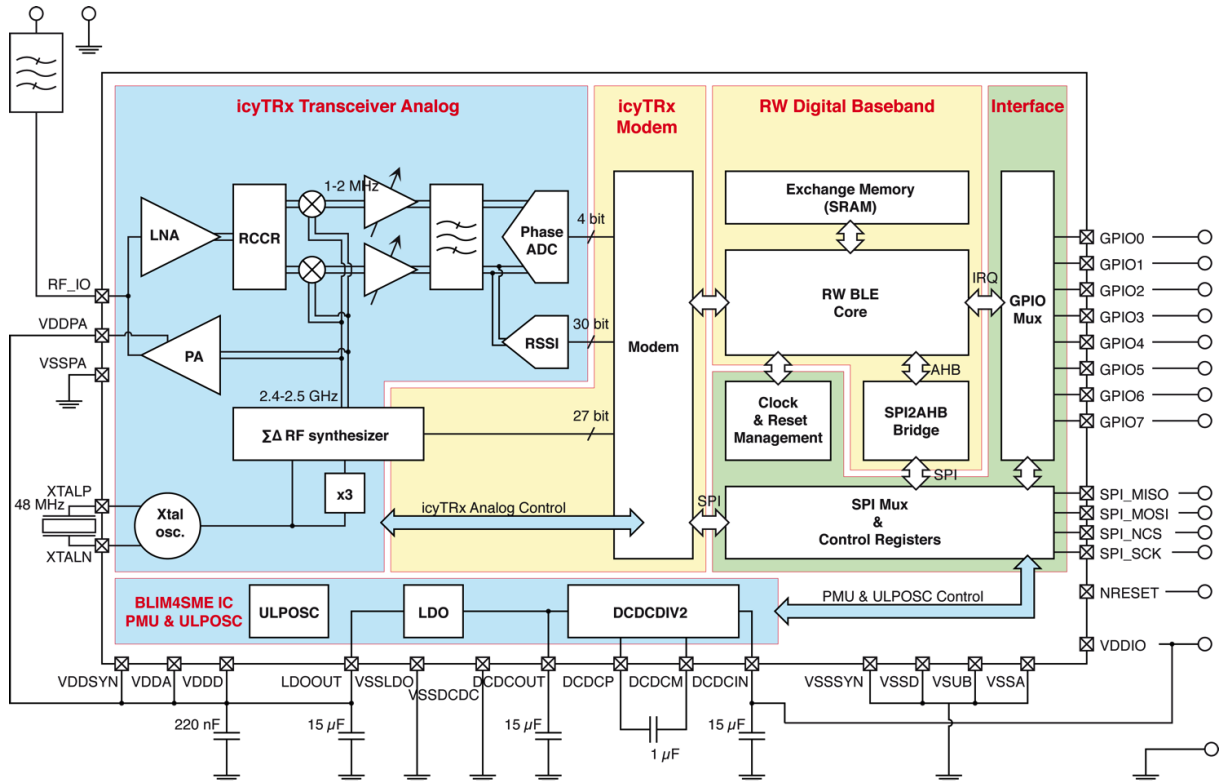


Figure 2: BLIM testchip block diagram.

The BLIM4SME circuit is mainly the assembly of existing transceiver IP from CSEM (namely *icyTRX-65*) and the protocol engine IP from RivieraWaves, with necessary modification for optimized co-operation and system-related development. In addition, some BLIM4SME-specific designs have been implemented in BLIM testchip.

The architecture of the BLIM4SME chip is composed by the following blocks:

- **RW digital baseband controller:** this provides the hardware part of Bluetooth® Low Energy 4.1 compliant stack from Link layer to (software part being implemented in companion MCU).
- **IcyTRX transceiver analog and digital modem:** this is the 2.4GHz RF radio block with the included modem.
- **Interface:** the access to the chip is done through a SPI bus. The communication is realized by with the RW sub-system. Moreover, in order to keep the power consumption on a minimum, the subsystems have to be turned off. In this case, the SPI slave of the two sub-blocks will not be available and the wake up may be sent via the SPI bus. For these reasons, a SPI multiplexer and the configuration static registers are present, in order to wake up the system quickly.
- **PMU:** this is the Power Management Unit including DC-DC conversion LDO voltage regulation and all-integrated retention voltage generation.

- **ULP Oscillator:** this is a low power oscillator. It is used to reduce the power consumption in the sleep mode of the Bluetooth® LE protocol, where the required accuracy is lower ($\pm 500\text{ppm}$) compared to the active mode ($\pm 50\text{ppm}$).
- **RF Oscillator:** this is a 48 MHz Xtal oscillator that is included in icyTRX IP. The clock signal of this oscillator is used as clock for the digital blocks (icyTRX and RW-BLE core), and as clock reference for the RF blocks of the 2.4 GHz radio. This 48 MHz clock can be output on one of IC interface for possible external use.

2.2 Testchip footprint and interfaces

The $\varnothing 95\ \mu\text{m}$ balls are aligned on a regular $200\ \mu\text{m}$ -pitched grid:

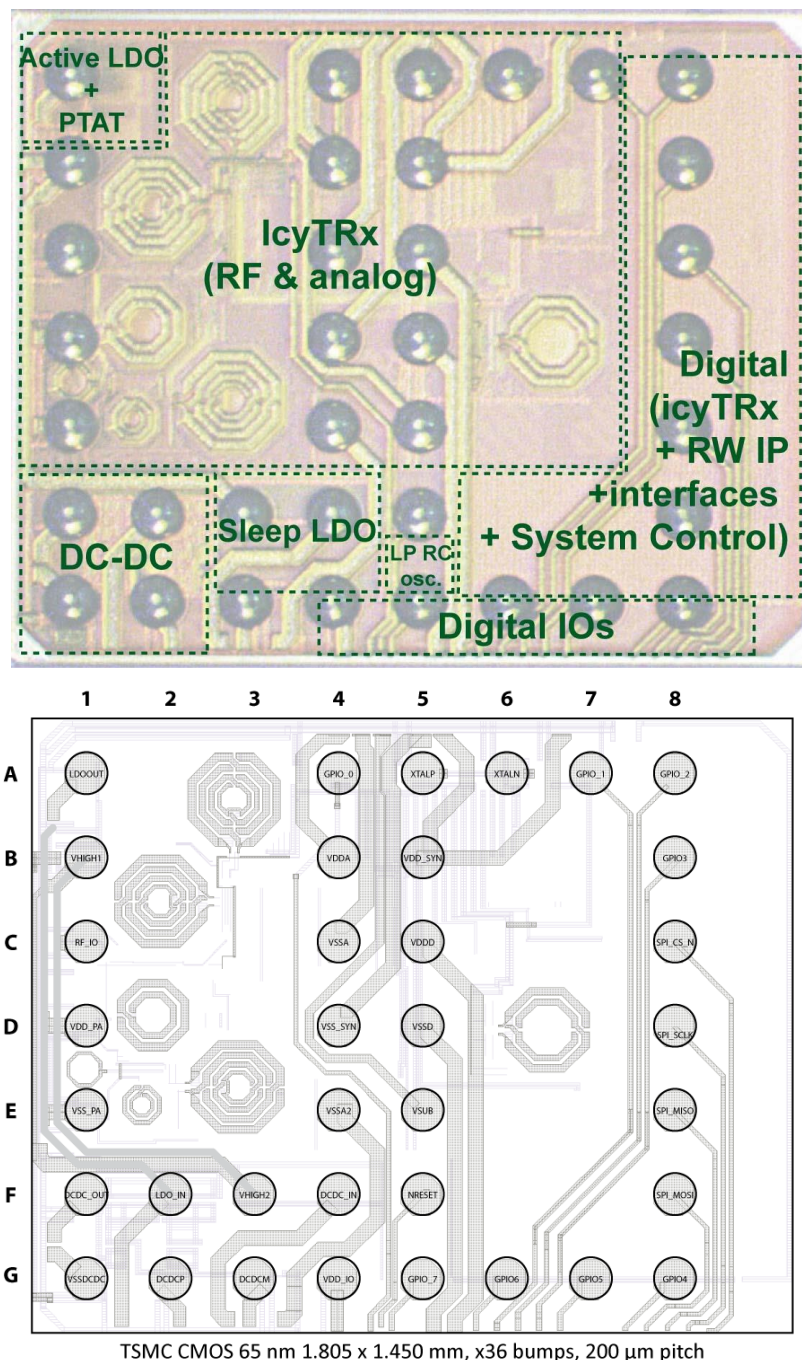


Figure 3: BLIM testchip die & floorplan (bottom view).

2.3 IC Interfaces

Ref	IO	Type	Description	Max. voltage
C1	RF_IO	A	50 Ω single-ended RF interface	1.32
A5	XTALP	A	Connection of quartz crystal resonator	1.32
A6	XTALN	A		1.32
A1	LDOOUT	A	Output of Low-Drop-Out Regulator	1.32
F2	LDOIN	A	Input of Low-Drop-Out voltage regulator	3.63
F4	DCDC_IN	A	Input of DC-DC capacitive voltage divider by 2	3.63
G2	DCDCP	A	Connection of flying capacitor of DC-DC capacitive voltage divider by 2	3.63
G3	DCDCM	A		3.63
F1	DCDC_OUT	A	Output of DC-DC capacitive voltage divider by 2	3.63
F5	NRESET	D	Reset of all chip, active at low level	3.63
A4	GPIO0	D	General-Purpose digital IOs on which are multiplexed different possible signal like IRQ, clkoc output, test signals, etc.	3.63
A7	GPIO1	D		3.63
A8	GPIO2	D		3.63
B8	GPIO3	D		3.63
G8	GPIO4	D		3.63
G7	GPIO5	D		3.63
G6	GPIO6	D		3.63
G5	GPIO7	D		3.63
E8	SPI_MISO	D	SPI Master-In-Slave-Out pin	3.63
F8	SPI_MOSI	D	SPI Master-Out-Slave-In pin	3.63
C8	SPI_CS_N	D	SPI Not-Slave-Select pin	3.63
D8	SPI_SCK	D	SPI Serial Clock pin	3.63
B1	VHIGH1	S	Voltage supply (biasing) of always-on blocks (voltage/current references, retention voltage LDO that also supplied ULP RC osc.)	3.63
F3	VHIGH2	S		
D1	VDD_PA	S	Positive supply of RF Power Amplifier	1.6
D4	VDD_SYN	S	Positive supply of RF synthesizer	1.32
B4	VDDA	S	Positive supply of analog	1.32
C5	VDDD	S	Positive supply of digital core	1.32
G4	VDDIO	S	Positive supply of digital IOs	3.63
E1	VSS_PA	S	Ground connection of RF power amplifier	0
D4	VSS_SYN	S	Ground connection of RF synthesizer	0
D5	VSSD	S	Ground connection of digital core and digital IOs	0
C4	VSSA	S	Ground connection of major par of analog (RF & associated LDO)	0
E4	VSSA2	S	Ground connection of always-on blocks and DC-DC	0
E5	VSUB	S	Collection of substrate current to ground	0
G1	VSSDCDC	S	Ground connection of DC-DC capacitive voltage divider by 2	0

Table 1: BLIM testchip IO list.

2.4 IP specification

Without precision, "Typ" specifications apply to a core voltage supply of 1.1V, temperature of 27°C, 50Ω RF load impedance, and "Min/Max" include PVT spread (7).

Parameters	Comments	Symb.	Min	Typ	Max	Units
Operating conditions and absolute maximum ratings						
Temperature	Operating temperature range	T _A	- 40	27	85	°C
ESD robustness (3)	Human Body Model measured on bumped naked dies	V _{ESD_HBM}	2.0	---	---	kV
ESD robustness (3)	Charged Device Model measured on bumped naked dies	V _{ESD_CDM}	200	---	---	V
Supply voltage	Core voltage (VDD_PA, VDDA, VDD_SYN, VDDD)		1.00	1.10	1.32	V
	IO voltage (all digital IOs, VDDHIGH, VDDIO, LDOIN, DCDC_IN, DCDCP, DCDCM, DCDC_OUT)		2.00	2.45	3.36	V
Leakage current	On VHIGH in sleep mode			0.6	2.0	μA
DC-DC capacitive divider by 2						
Supply voltage			2.0	2.45	3.63	V
Output current	Active mode		0.001	10	20	mA
Quiescent current	Active mode, without load			20		μA
Peak input current	Input capacitor supplied through 1 Ω resistor			TBM	100	mA
Switching frequency				0.5		MHz
Voltage dropout	10 mA output current			120		mV
Flying capacitor			220	1'000		nF
Output capacitor			1	15		μF
Startup time	No load, hibernate to active mode, 2.4 V input, 2.2 V output			TBM		μs
LDO						
Supply voltage			1.0	1.1	1.68	V
Regulated voltage	FF, 1.0-1.68 V Brownout at:		0.9			V
	TT, 1.1-1.68 V Brownout at:		1.0	1.05		V
	SS, 1.2-1.68V Brownout at:		1.050 1.1			V
Current load			0.1	10'000	20'000	μA
Quiescent current	Load-independent part.			10		μA
External capacitor			1	15		μF

Parameters	Comments	Symb.	Min	Typ	Max	Units
Ultra-Low-Power all-integrated oscillator						
Oscillator frequency			25	32	45	kHz
Tuning step	Without $\Sigma\Delta$ modulation of LSB			0.1		%
Temperature accuracy				4		%
Allan deviation	$t^{-0.5}$ to floor corner time			0.1		s
	Floor			5		ppm
Current consumption	On VHIGH			300		nA
General radio specifications						
Compliant with	Bluetooth® LE (1), ETSI EN 300 440, ETSI EN 300 328, FCC CFR47 part 15..					
Supply voltage	VDDD, VDDA, VDD_SYN, VDD_PA		1.00	1.10	1.32	V
RF input impedance	Single ended	Z_{IN}	---	50	---	Ω
Input reflection coefficient	All channels	S_{11}	---	---	- 8	dB
Input power without damaging IC	Indicative rating		---	---	+18	dBm
XO & clock specifications						
Xtal frequency	Fundamental	f_{XTAL}	48.0000			MHz
Supported Xtal parameters	Equiv. series Res.	ESR_{XTAL}	20		80	Ω
	Differential equivalent load capacitance	CL_{XTAL}	6.0	8.0	10.0	pF
Settling time	Startup to RF functionality		---	0.5	1.5	ms
Synthesizer specifications						
Frequency range	Supported carrier frequencies	F_{RF}	2360	---	2500	MHz
Rx frequency step	RX mode frequency synthesizer resolution		---	---	100	Hz
Tx frequency step	TX mode frequency synthesizer resolution		---	---	600	Hz
PLL Settling time, RX	RX mode	t_{PLL_RX}	---	15	25	μ s
PLL Settling time, TX	TX mode, BLE modulation	t_{PLL_TX}	---	5	10	μ s
Receive mode specifications						
Current consumption from V_{DDA}	BLE Modulation. Continuous operation (100% D.C.) (4)	I_{VDDARX}	--	4.7	6.8	mA
Current consumption from V_{DDD}	BLE Modulation. Continuous operation (100% D.C.).	I_{VDDDRX}	--	0.7	1.2	mA
BLE Sensitivity	0.1% BER @ 1Mbps. BLE (5)(6)		- 91	- 97	---	dBm
2 Mbps Sensitivity	0.1% BER @ 2Mbps MSK and GFSK (BT=0.5, fdev = data rate/4) (5)(6)		- 89	- 95	---	dBm
RSSI effective range	Without AGC		---	60	---	dB
RSSI step size			---	2.4	---	dB
RX AGC range			---	48	---	dB
RX AGC step size	Programmable		---	6	---	dB
Max usable signal level	(6)		0	5	---	dBm

Parameters	Comments	Symb.	Min	Typ	Max	Units
Transmit mode specifications						
Current consumption from V_{DDA}	"0 dBm" output power setting, i.e. for a fixed V_{DD_PA} of 1.1V. (5)	$I_{VDDATX0}$	--	7.7	8.9	mA
Current consumption from V_{DDA}	Minimum output power setting (-17dBm). (4)	$I_{VDDATX-20}$	--	3.8	5.2	mA
Current consumption from V_{DDD}	BLE Modulation. Continuous operation (100% D.C.).	I_{VDDDTX}	--	0.75	1.2	mA
Transmit power range	BLE or 802.15.4 OQPSK		- 17		0.5	dBm
Transmit power step size	Full band.		---	2	---	dB
Transmit power accuracy	"0 dBm" mode. All PT corners. Full band. Relative to the typical value.		- 1.1	---	+ 1.5	dB
Transmit power accuracy	"0 dBm" mode. T=27°C. All process corner. Full band. Relative to the typical value.		- 0.4	---	+ 0.9	dB
Power in 2 nd harmonic	"0 dBm" mode. 50 Ω for "Typ" value. PT for "Max" value (2)		---	-26	-20	dBm
Power in 3 rd harmonic	"0 dBm" mode. 50 Ω for "Typ" value. PT for "Max" value (2)		---	-27	-22	dBm
Power in 4th harmonic	"0 dBm" mode. 50 Ω for "Typ" value. PT for "Max" value.		---	-45	-35	dBm

Table 2: RF IC IP specifications**Notes:**

- 1) Bluetooth® 4.2. Measured according to Bluetooth® Low Energy Test Specification RF-PHY.TS/4.0.1. Test Report available on request.
- 2) Except for harmonics of carrier frequency (c.f. above table), to be filtered (e.g. with selective antenna design)
- 3) According to TSMC I/O's library. Custom pads (i.e. RF) not yet tested in 65nm, but ESD protection topology validated on icyTRX 90nm version.
- 4) PTAT behavior of analog bias.
- 5) Signal generated by RF tester.
- 6) Sensitivity and max signal level specifications correspond to 0.1% BER on received signal.
- 7) PVT = IC Process, Voltage & Temperature.

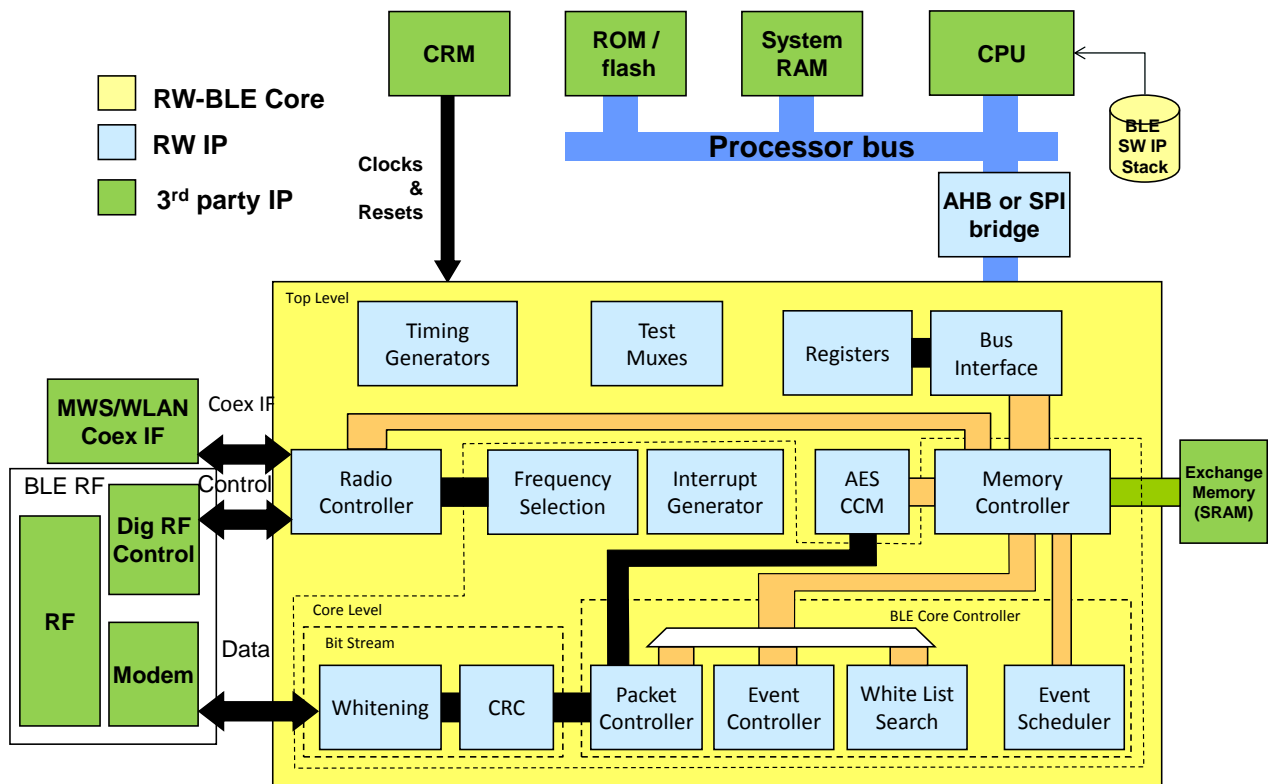


Figure 4: RW IP block diagram.

The RW-BLE Core has the following features:

- Bluetooth® Low Energy (a.k.a Bluetooth® Smart) 4.2 Specifications compliant.
This is the latest available specification from the Bluetooth® SIG, as of the writing of this document. It supports all of the mandatory and optional features of the Bluetooth® Low Energy 4.2 Specification.
- Support AMBA AHB bus
The bus interface converts the signals from the external processor bus to the internal format. It is dedicated to the standard AMBA2 AHB bus of the ARM processor.
It is to be noted that for the purpose of BLIM4SME project, as there is no processor in the IC designed, an SPI interface will be used instead of AHB in order to connect the IC to an external MCU chip.
- All packet types (Advertising / Data / Control).
All the packets defined in the Bluetooth® Smart specification are handled directly in the digital baseband without a need for participation from the MCU. This includes all roles for the different packet types (master, slave, initiator, advertiser, scanner, ...)
- Encryption (AES / CCM)
The digital baseband supports the AES-CCM encryption and decryption, should the packets contain encrypted data as specified by the standard.
- Bit stream processing
The bit stream processing is performed for packet transmission and reception:
 - For transmission: collecting of different parts of the packets, encryption and encrypted MIC appending, serialization of the transmitted data, CRC calculation, and whitening computation.

- For reception: correlation of the synchronization word, synchronization detection during a generated window, de-whitening, CRC checking, de-serialization, decryption and MIC checking, and storage of the data into the Exchange Memory
- Frequency-hopping calculation
The frequency selection block calculates automatically the channel frequency to be used for the next packet to be transmitted or received over the air, based on a pseudo random algorithm specified in the Bluetooth® standard and on some parameters given by the software. It supports three main frequency-hopping schemes composed by:
 - 37 data channels (index in [0:36] range)
 - 3 advertising channels (index in [37:39] range)
 - Test modes: any of the 40 channels [0:39], to be set manually

S-FORMAT	Channel Type
Master Connect	Data Channel
Slave Connect	Data Channel
Advertiser	Advertising Channel
Passive Scanner	Advertising Channel
Active Scanner	Advertising Channel
Initiator	Advertising Channel
Tx Test Mode	n/a ⁽¹⁾
Tx Test Mode	n/a ⁽¹⁾
Tx/Rx Test Mode	n/a ⁽¹⁾

Table 3: Frequency Hopping Scheme Selection

- TDMA events formatting and synchronization
When several Bluetooth® links are established at the same time, the digital baseband handles the TDMA (Time Division Multiple Access) scheduling and operation, being able to share efficiently the allocated time slots between the different links.
- All device classes support (Broadcaster, Central, Observer, Peripheral)
These are the four different classes of Bluetooth® Low Energy devices, either
 - Broadcaster: the device is only performing transmission over the Bluetooth® link, not expecting responses
 - Observer: the opposite of the Broadcaster, the device is only set to receive Bluetooth® packets, and does not transmit
 - Central: the device is central in a Bluetooth® connection network and manages several links to several peripherals, acting as master
 - Peripheral: the device is the slave of a Bluetooth® connection, connected to a central device
- Low power modes supporting 32.0kHz or 32.768kHz low-power clock frequencies.
When in active mode, the RW-BLE Core baseband is running on the main clock of the system, which can be as low as 8MHz. When in low power mode, most of the RW-BLE Core can be “gated”, meaning the system clock can be stopped in order to reduce the power consumption. The power supply of this portion could also be switch off in order to reduce even further the power consumption. However, a small portion of the RW-BLE Core needs to remain active in order to maintain a time base. This small portion can run on a low power

clock (32.0KHz or 32.768KHz) to consume less. It can also be merged with the RTC (Real Time Clock) of the chip.

- DFT included, accepted by major ATPG tools.
The digital baseband has been designed for, and is suited to compatibility with, all the major tools used for ATPG (Automatic Test Pattern Generation), which insert the necessary test fixtures and generates production test vectors for automated integrated circuit production testing.
- Simple, and optimized interface to RW-BLE Software
The communication between the RW-BLE core and the software is depicted in Figure 9. The Exchange Memory contains buffers to be transmitted or received by the core. It also contains control parameters to manage the packet format and its features, as well as some receive status (CRC error, SN/NESN error, etc...). Registers are used for static control parameters and real-time information. Interrupts are used to synchronize the software with the core.
- Low power consumption
The RW-BLE core design has been optimized in order to minimize the peak power consumption in active mode (less than 100uA at 8MHz), and the power consumption in low power mode (less than 1uA).
- Low frequency of operation
The digital baseband can perform down to an 8MHz clocking frequency in active mode.

The RW-BLE-Core requires a small SRAM to store transmit and received data as well as the different parameters for the connection. The size of this memory shall be 4 KBytes, which allows behaving as a central device with up to 7 active connections simultaneously.

3 RF IPD component and associated antenna

The RF IPD component and associated miniature antenna does not need any ground plane or ground plane opening areas to function.

The 1.5 x 1.2 x 0.3 mm RF IPD component is based on thin film technologies over silicon wafer. It realizes a filtering and an RF impedance matching between a 50 Ω single-ended RF interface and the antenna.

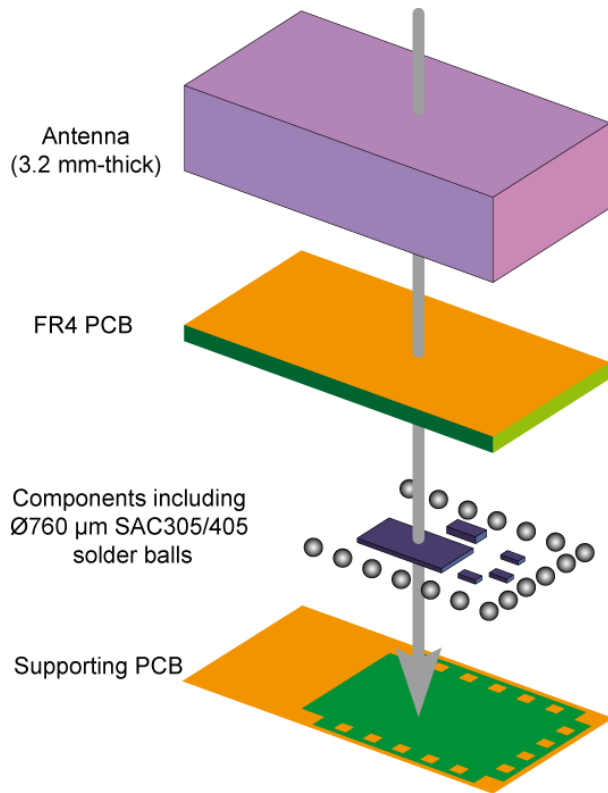


Figure 5: Modules mechanical architecture.

Parameters	Comments	Symb.	Min	Typ	Max	Units
Port to transceiver	Single-ended			50		Ω
Bandwidth			2'400		2'484	GHz
Rejection	876 - 959 MHz (GSM)			40		dB
	4'800 – 4'968 (2 nd harmonic)		30			
	5'150 - 5'725 MHz (WLAN)			15		dB
Gain	(1)(2)		-9		-2	dBi

Table 4: Specification of RF IPD component and associated miniature antenna.

Notes:

- 1) Gain is the total module gain including all the component and interconnection loss from transceiver to the air.
- 2) Spread specification is associated to contexts describes in table below:

	Free space (dBi)	On 100 x 300 mm metal (dBi)	On body (dBi)
27x55mm application board	-6.5	-2.5	-4.5
25x25mm application board	-9.5	-2.5	-7.5

Table 5: Gain spread contexts, values at ± 0.5 dB.

Antenna radiation is approximately uniform (depending also on supporting PCB) as illustrated in Figure 6 below:

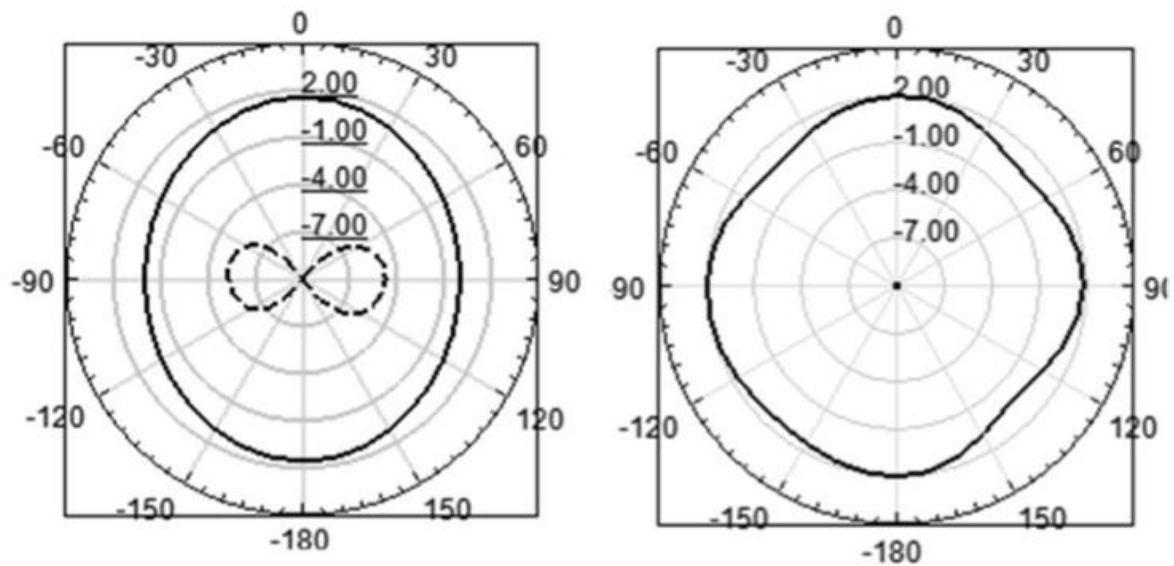


Figure 6: Simulated module radiation pattern in free space, $\phi = 0^\circ$ (left), $\phi = 90^\circ$ (right), solid curve represents D_ϕ and dashed D_θ .

4 COTS Module and BLIM Module

4.1 Footprint and interfaces common to both modules

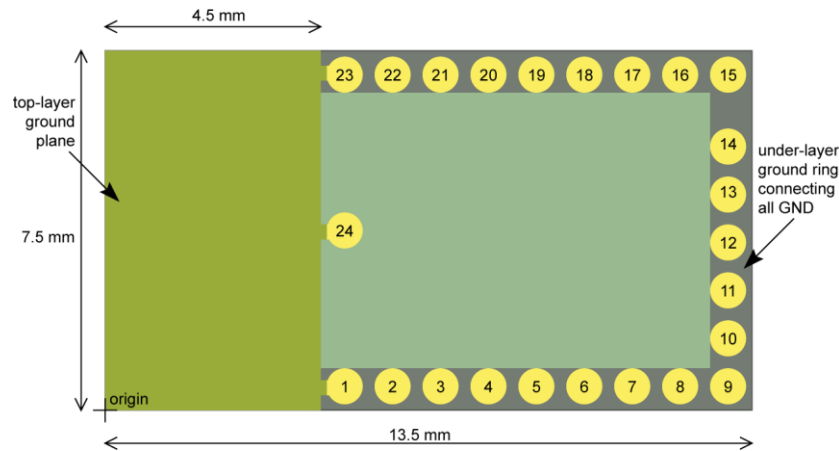


Figure 7: BLIM module footprint (top view).

Ball	IO Type	Typical functions	Description	X	Y
1	S	GND2	Module ground connection	5.00	0.50
2	DIO	UART1_TX	A priori main UART for communication with host controller (general purpose analog or digital IO)	6.00	0.50
3	DIO	UART1_RX		7.00	0.50
4	DIO	ADC_IN2		8.00	0.50
5	DIO	ADC_IN3	Analog input or General purpose analog or digital IO	9.00	0.50
6	DIO	I2C_SCL	I2C interface	10.00	0.50
7	DIO	I2C_SDA		11.00	0.50
8	DIO	SPI_NSS	SPI interface Not-Slave-Select	12.00	0.50
9	S	GND1	Module ground connection	13.00	0.50
10	DIO	GPIO0	General purpose GPIO	13.00	1.50
11	DIO	RESET	RESET active high for COTS, low for BLIM	13.00	2.50
12		VPP	GPIO for BLIM module	13.00	3.50
13	S	GND3	Module ground connection	13.00	4.50
14	S	VBAT3V	2.4-3.6 V positive voltage supply	13.00	5.50
15	S	GND4	Module ground connection	13.00	7.00
16	DIO	SPI_SCK	SPI interface Serial Clock	12.00	7.00
17	DIO	SPI_MISO	SPI interface Master-In Slave-out	11.00	7.00
18	S	VBAT1V	Low-voltage positive supply	10.00	7.00
19	DIO	SWDIO	Serial Wire Debug interface data (JTAG - similar)	9.00	7.00
20	DIO	SWCLK	Serial Wire Debug interface clock (JTAG - similar)	8.00	7.00
21	DIO	SPI_MOSI	SPI interface Master-Out Slave-In	7.00	7.00
22	S	GPIO1	General purpose GPIO (e.g. for SPI chip select)	6.00	7.00
23	S	GND5	Module ground connection	5.00	7.00
24	S	GND6		5.00	3.75

Table 6: Modules pinning with coordinate in mm.

BLIM module being footprint-compatible with COTS module, the table below lists how the modules interfaces are mapped to internal MCU, on KL15P35M48SF0 Cortex M0+ from Freescale for BLIM module and on DA14580 for COTS module:

Ball	MCU pin mapping		Signal functions (Typical in bold)
	COTS	BLIM	
1	GND	GND	GND2
2	P0_0	PTE20	UART1_TX / ADC_IN0 / PWM0
3	P0_1	PTE21	UART1_RX / ADC_IN1/ PWM1
4	P0_2	PTE16	ADC_IN2 /GPIO2/ PWM2
5	P0_3	PTE17	ADC_IN3 / GPIO3/ PWM3
6	P0_4	PTE1	I2C_SCL / UART2_Rx
7	P0_5	PTE0	I2C_SDA / UART2_Tx
8	P0_6	PTD4	SPI_NSS
9		GND	GND1
10	P0_7	PTE18 ?	GPIO0 / ADC_IN4
11	RST	PTA20 & NRESET	RESET
12	VPP	PTE30	VPP
13		GND	GND3
14	VBAT3V	VDDA & VDD	VBAT3V
15		GND	GND4
16	P1_1	PTD5	SPI_SCK
17	P1_2	PTD7	SPI_MISO
18	VBAT1V	LDO_IN	VBAT1V
19	P1_5	PTA3	SWDIO
20	P1_4	PTA0	SWCLK
21	P1_3	PTD6	SPI_MOSI
22	P1_4 (=SWCLK)	PTE19	GPIO1
23		GND	GND5
24		GND	GND6

Table 7: Internal MCU signal mapping.

This assure, with different Hardware Abstraction Layers, functional compatibility between modules:

The functionality is Bluetooth® Low Energy communication module with UART interface (SPI or I2C could also be considered). Limited application or functions (co-processor of the main one) can also be implemented with limited analog (10-bit ADC, PWMs) and digital interfaces (SPI, I2C, GPIOs).

4.2 COTS module

The COTS Module is based on a DA14580 Dialog BLE SoC, common RF IPD component and associated miniature antenna common to both modules (c.f. section 4.1) and some solder balls.

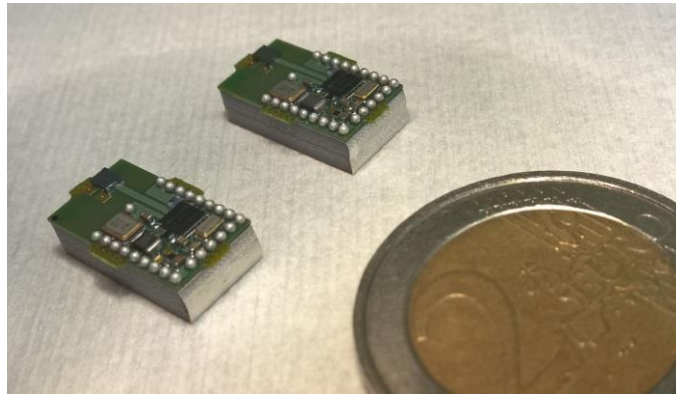


Figure 8: 13.5 x 7.5 x 4 COTS Module, bottom view.

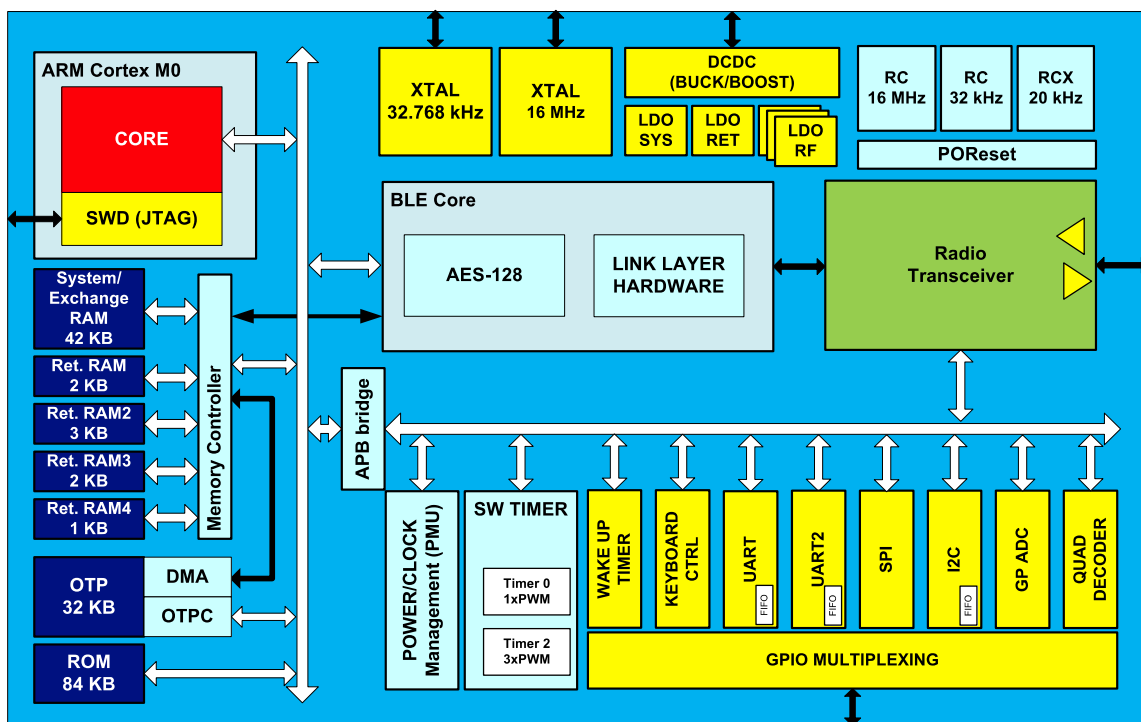


Figure 9: DA14580 block diagram

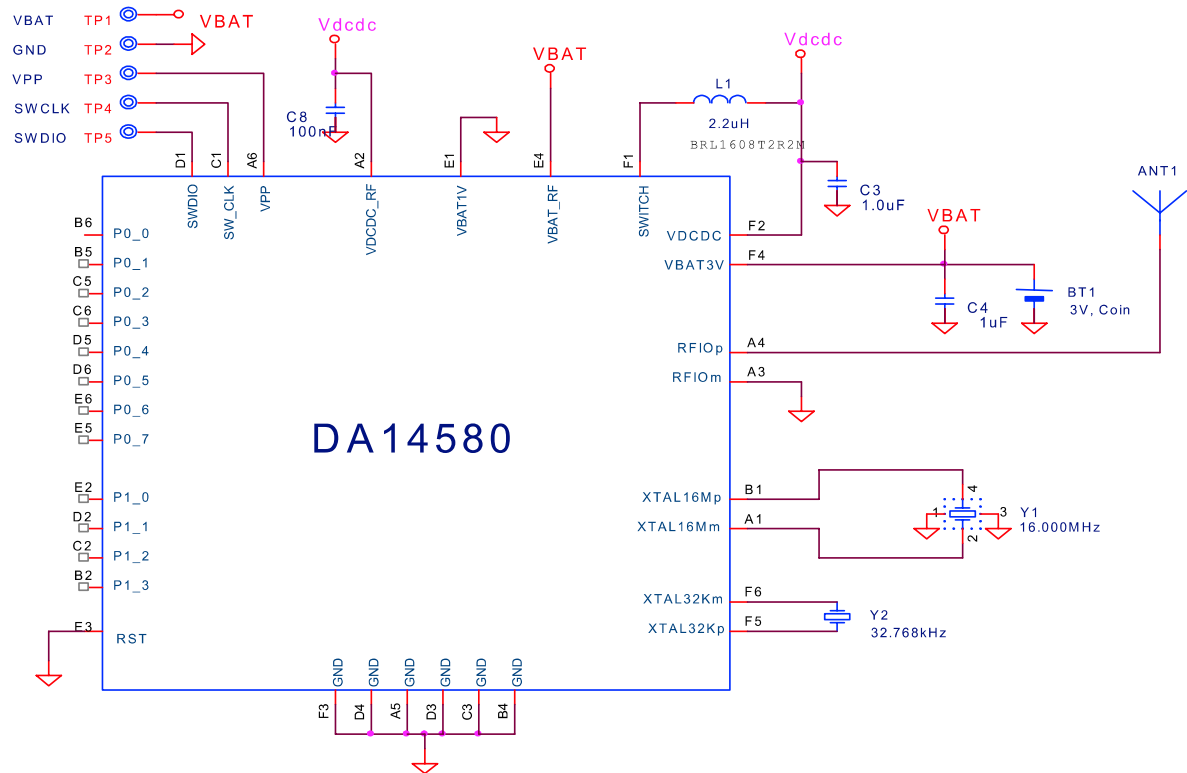


Figure 10: Schematic of COTS module.

Description	Quantity	Provider
DA14580 WLCSP	1	Dialog
Xtal 16 MHz ABM11	1	Abrakon
Xtal 32.768 kHz ABS06	1	Abrakon
1 μ F X5R 0402	2	AVX
2.2 μ H, 350 mA, 0.55 Ω	1	TDK
100 nF 6.3 V ceramic	1	Samsung
IPD /mm ²	1.8	VTT
SAC405 Spheres Ø0.760mm	25	Capling
Duroid 5870 /mm ²	101	Rogers
FR4 PCB, 4-6 layers /mm ²	101	

Table 8: COTS module Bill-of-Materials.

4.3 BLIM module

The BLIM Module is based on the BLIM Testchip and a Cortex M0+ companion MCU, common RF IPD component and associated miniature antenna common to both modules (c.f. section 4.1) and some solder balls

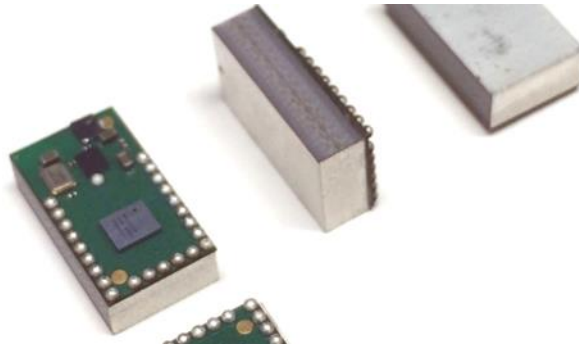


Figure 11: 13.5 x 7.5 x 4 BLIM Module, bottom view.

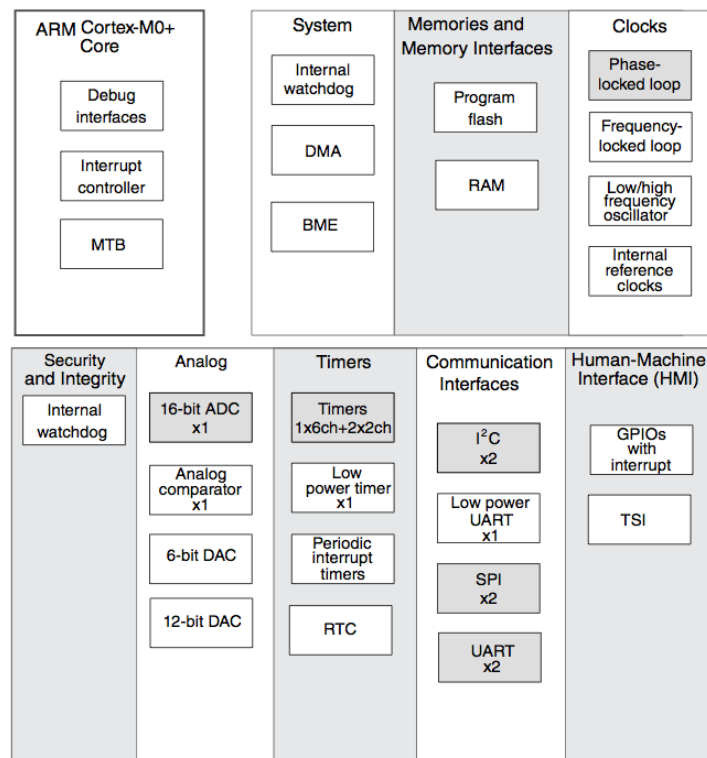


Figure 12: KL15P35M48SF0 functional block diagram.

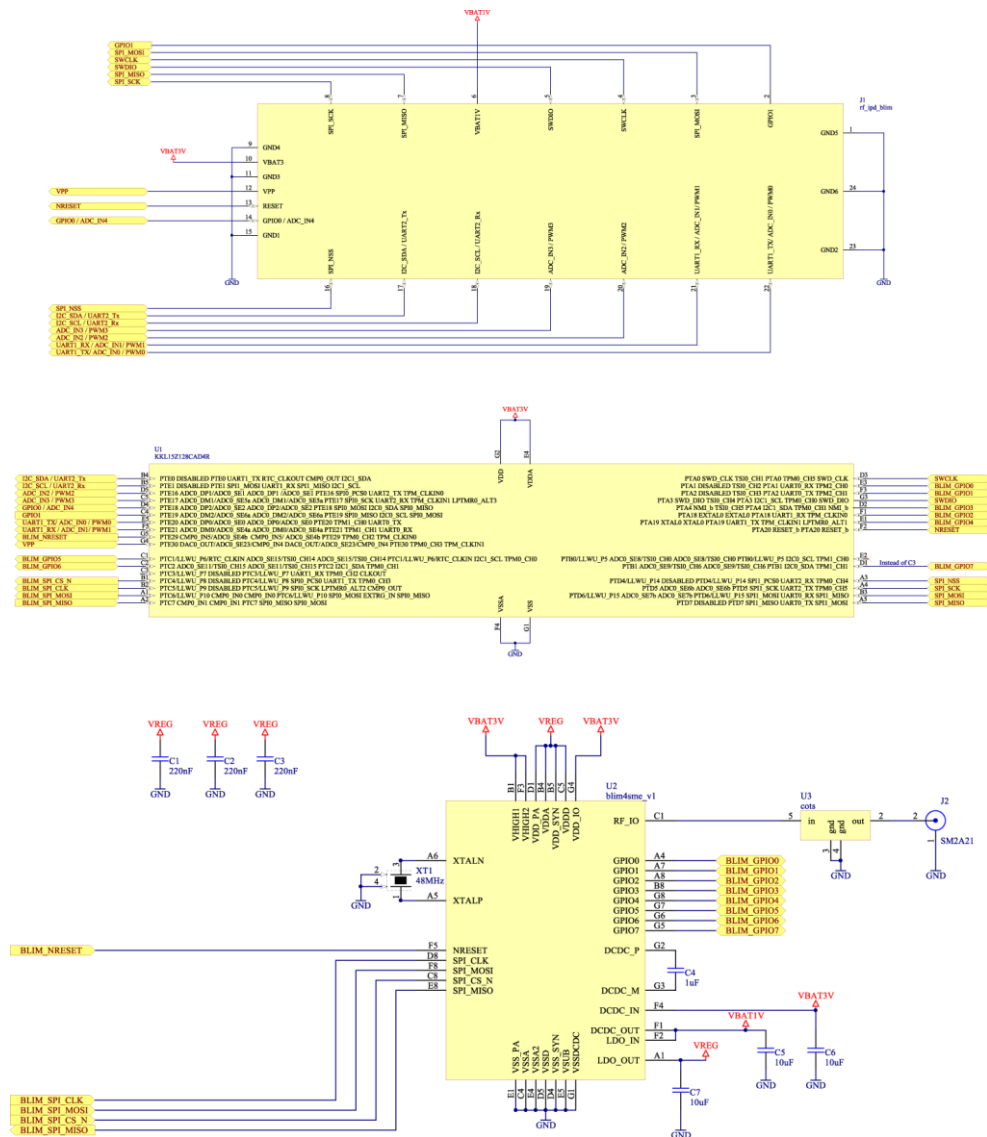


Figure 13: BLIM module schematic (top: footprint, middle: Cortex MCU, bottom: BLIM Testchip).

Description	Quantity	Provider
BLIM IC /mm ²	2.6	TSMC
ARM cortex M0 128kB KL15P35M48SF0	1	Freescall
48 MHz Xtal 7 pF	1	AVX Corp.
10 µF 6.3 V 0402 ceramic	3	TDK
1 µF 6.3 V 0201 ceramic	1	TDK
220 nF 6.3 V 01005 ceramic	3	AVX Corp.
IPD /mm ²	4	VTT
Duroid 5870 /mm ²	101	Rogers
FR4 PCB, 4-6 layers /mm ²	101	Rogers
SAC405 Spheres Ø0.760mm	25	Capling

Table 9: COTS module Bill-of-Materials.

5 Generic Module

The Generic Module embeds one of the COTS or BLIM module with several sensors (temperature, humidity, barometer, 3D accelerometer and compass, ultrasonic microphone) and a microSD socket (typ. for flash card memory). This Generic Module is pin-to-pin compatible with a Zigbee module presently used in PRISMA products.

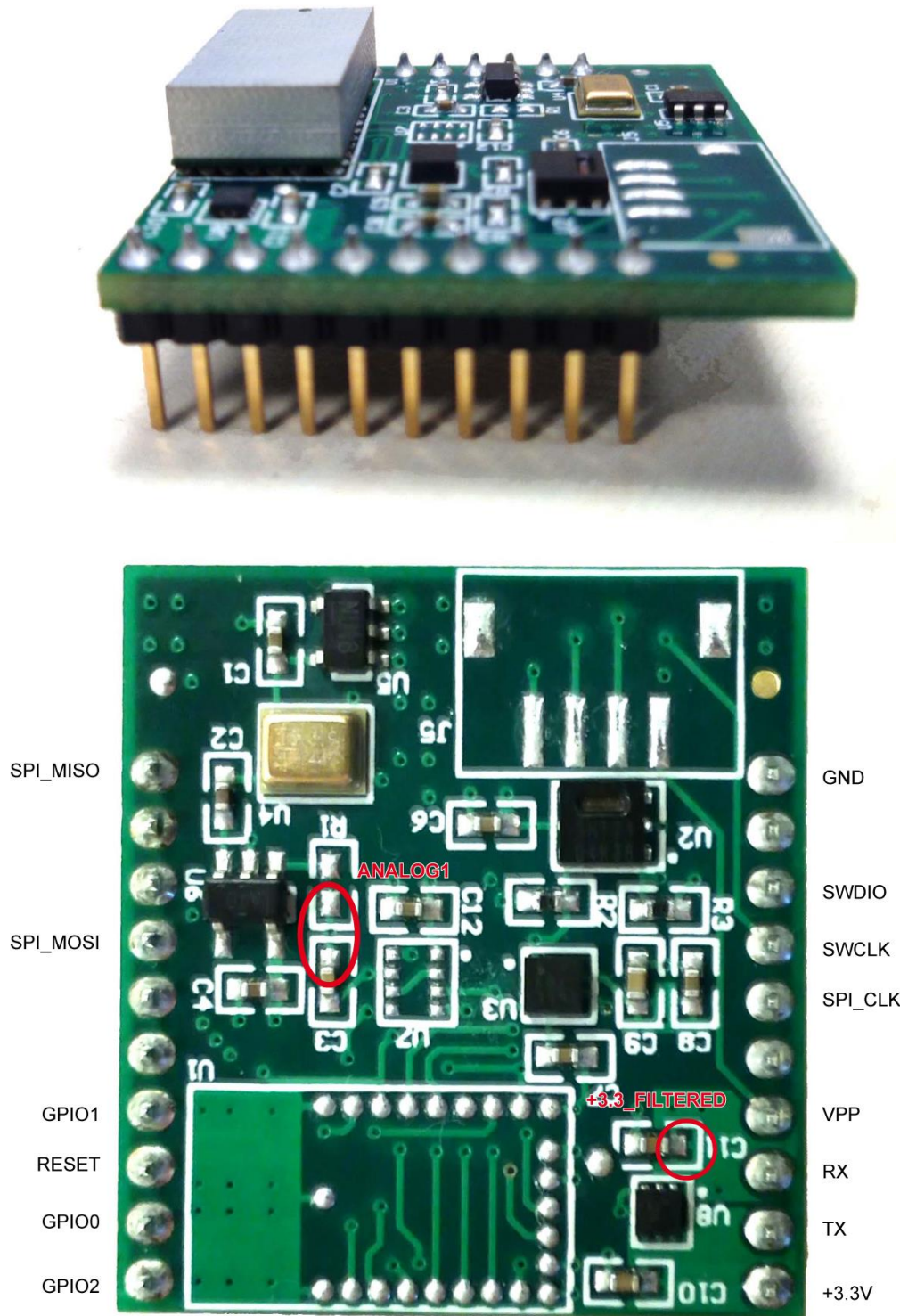


Figure 4.1: 27 x 25 mm Generic Module (module footprint on bottom-left).

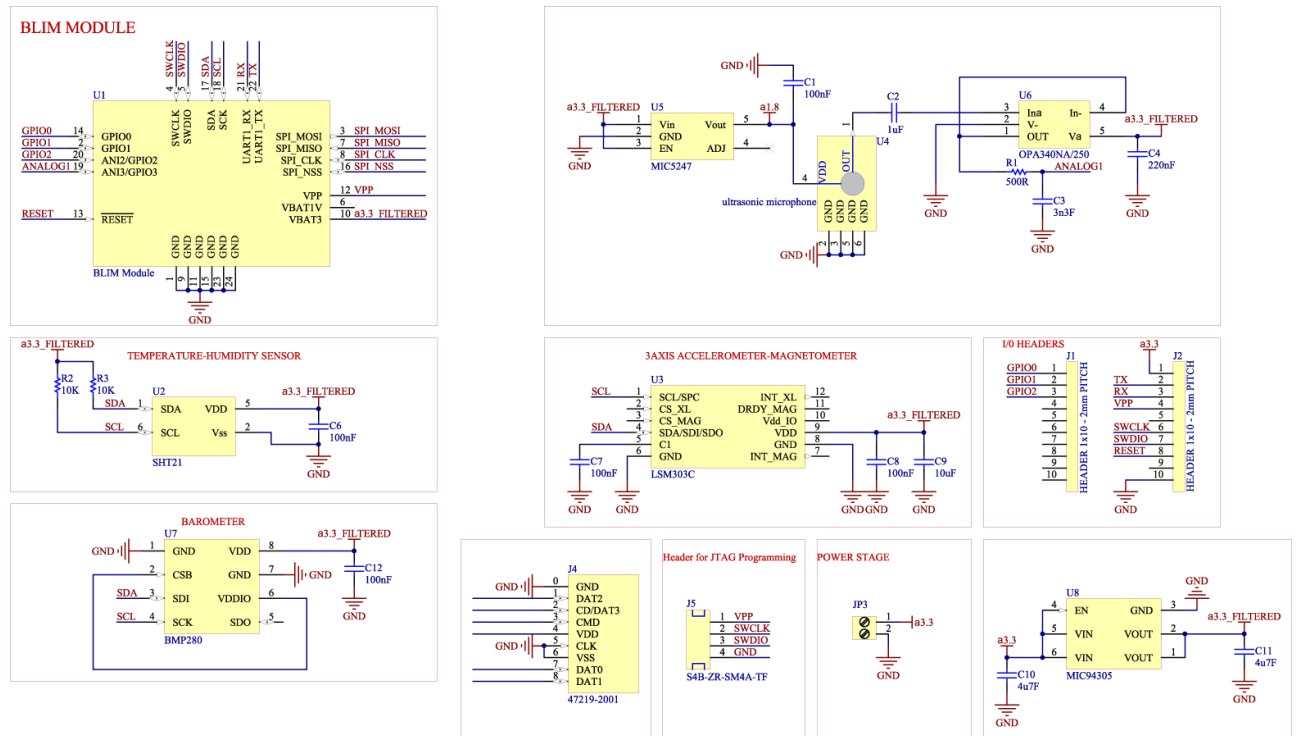


Figure 14: BLE Generic module schematic.

Designator	Description	Footprint	Quantity	Value	Ordering
C1, C6, C7, C8, C12	Capacitor Ceramic SMT	0402	5	100nF	GRHM155H71C104KA88D
C2	Capacitor Ceramic SMT	0402	1	1uF	C1005X5R1A105M050B
C3	Capacitor Ceramic SMT	0402	1	3n3F	GRHM155H72A332KA01D
C4	Capacitor Ceramic SMT	0402	1	220nF	GRHM155H6YA224KE01D
C9	Capacitor Ceramic SMT	0402	1	10uF	GRHM155H6UJ106ME44D
C10, C11	Capacitor Ceramic SMT	0402	2	4u7F	GRHM155H6UJ475ME47D
J1, J2		HEADER 1X10 - 2mm PITCH	2		
J4		MOLEX-47219-2001	1		47219-2001
J5	RIGHT ANGLE CONNECTOR 4POS, 1.5MM, SMT	S4B-ZR-SM4A-TF	1		S4B-ZR-SM4A-TF(LF)(SN)(P)
JP3	JST wire to board connector 1,5mm pitch	B2B-ZR SMT	1	B2B-ZR	B2B-ZR
R1	Resistor SMT	0402	1	500R	
R2, R3	Resistor SMT	0402	2	10K	RK73B1ETTP103J
U1		BLIM_Module	1		
U2	Temperature & Humidity Sensor	SHT21	1		SHT21/ 403-SHT21 Mouser
U3	Ultra-compact high-performance eCompass module: 3D accelerometer and 3D magnetometer	LGA-12 2x2x1 mm	1		LSM303CTR
U4	low power, bottom port silicon microphone	SPU0410LR5H-QB	1		SPU0410LR5H-QB
U5	TSUMA Low-voltage linear regulator	TSOT-23.5	1		576-3007-6-ND
U6	Operational Amplifiers - Op Amps Single-Supply Rail-to-Rail	SOT-6.5	1		OPA340NA/250
U7	Pressure Sensors Digital Barometer 2.7uA, 300-1200hPa	BMP200	1		BMP200
U8	MIC500mA Switch with Ri	DFN-6 1.6x1.6mm	1		MIC94305YMT T5

Table 10: BLE Generic Module Bill-of-Materials.

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